Getting Pin Numbers On a Design

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May 13, 2014

Abstract

A design's pin number information is not typically recorded in a consistent manner.

Saving pin number information in a VHDL source file provides a way to address this issue.

The eightolives Workspaces Desktop DesignTool has features to help capture and manage pin information.

The Problem

- Different FPGA vendors specify device pinouts using different proprietary constraint file formats (i.e. .ucf files)
- Tools that translate circuit card schematics to VHDL don't capture the pin information.

Proposed Solution

- Capture pin information in the design's top level VHDL file using the format prescribed for Boundary Scan Descriptions (IEEE 1149.1)
  - FPGA vendors provide BSDL files for their various packages
  - Schematics saved as EDIF files contain pin information
  - Use the eightolives Workspaces Desktop tool to help integrate this information and create the VHDL file

Extract from Texas Instruments SN74LVTH18502ALS BSDL File

```
entity sn74lvth18502a is

    generic (PHYSICAL_PIN_MAP : string := "UNDEFINED");

    port (OEAB_NEG1:in bit;

          OEAB_NEG2:in bit;

          OEBA_NEG1:in bit;

.....

    use STD_1149_1_1990.all; -- Get standard attributes and
definitions



    attribute PIN_MAP of sn74lvth18502a : entity is
PHYSICAL_PIN_MAP;
```

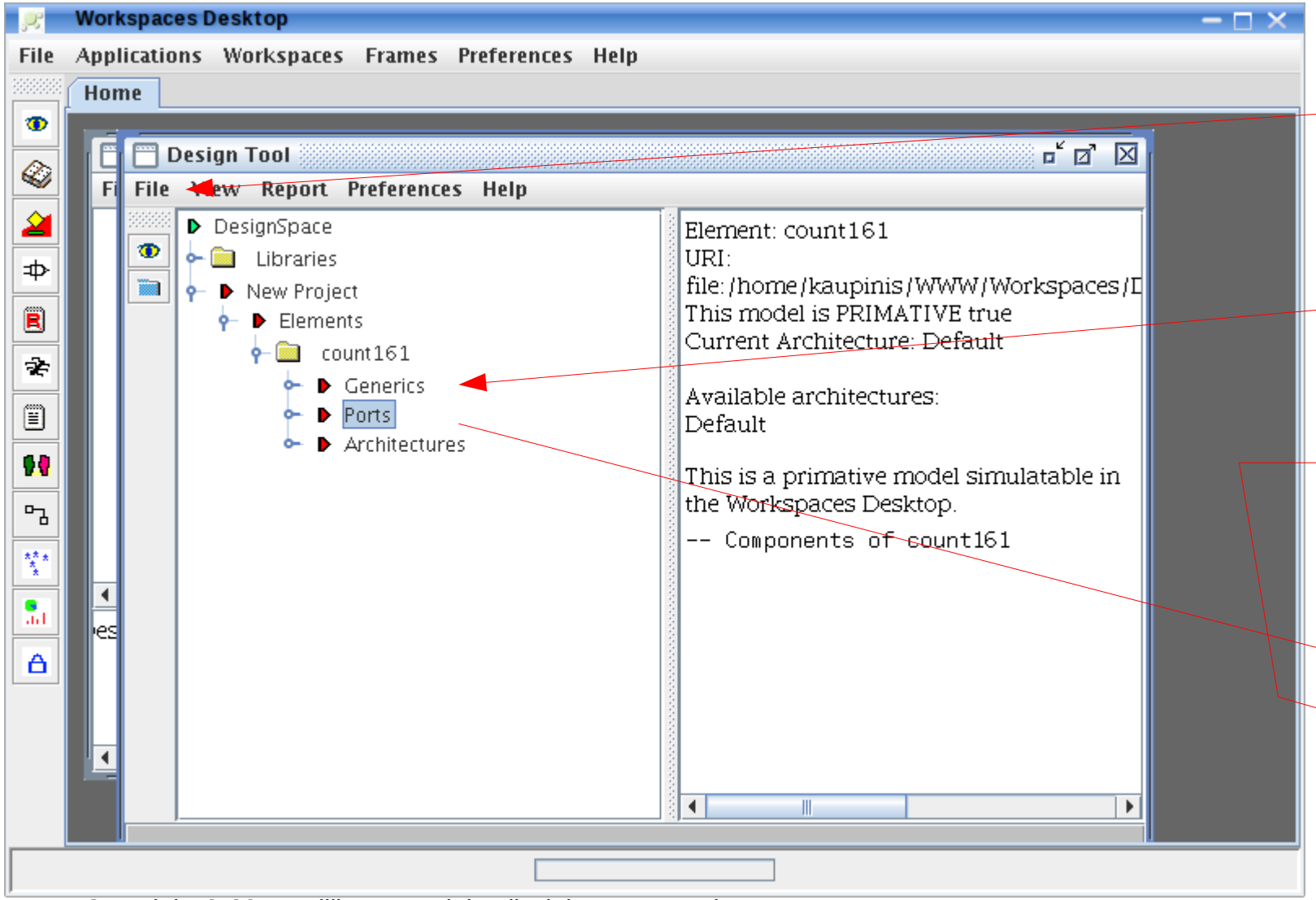
```
constant PM : PIN_MAP_STRING := "OEAB_NEG1:62,
OEAB_NEG2:21,"&

              "OEBA_NEG1:53, OEBA_NEG2:30,"&

              "LEAB1:60, LEAB2:22, LEBA1:54, LEBA2:28,"&

              "CLKAB1:59, CLKAB2:23, CLKBA1:55,  CLKBA2:27,"&

              "A1:(63,64,1,2,3,5,6,7,8),"&

              "A2:(10,11,12,14,15,16,17,18,19),"&

.....

              "B2:(51,50,49,48,46,45,44,43,42),"&

              "GND:(6,13,23,30,40,47,57,64),"&

              "VCC:(2,19,36,53),"&

              "NC:(1,18,35,52),"&

              "TCK:37, TDI:34, TMS:68, TDO:3 ";
```

The pin information is contained in a VHDL String listing signal name and pin number

How does Workspaces Desktop Help?

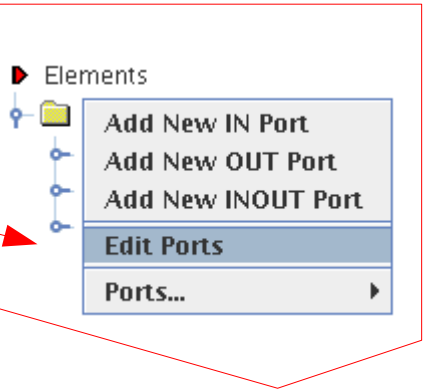
- Top level Port names of an FPGA design don't match the Port names used in the BSDL file
  - Workspaces Desktop captures pin data from BSDL, ucf and edf files
  - Workspaces Desktop can merge pin and port data using menu commands
    - Group Intersect by Name (design file and constraint file)
    - Group Union by Pin (design file and BSDL file)
- There may be no electronic source of pin information so you have to specify it manually
  - Edit Ports window is a table for manual pin entry

To manually add Pin Numbers, first read in your design file

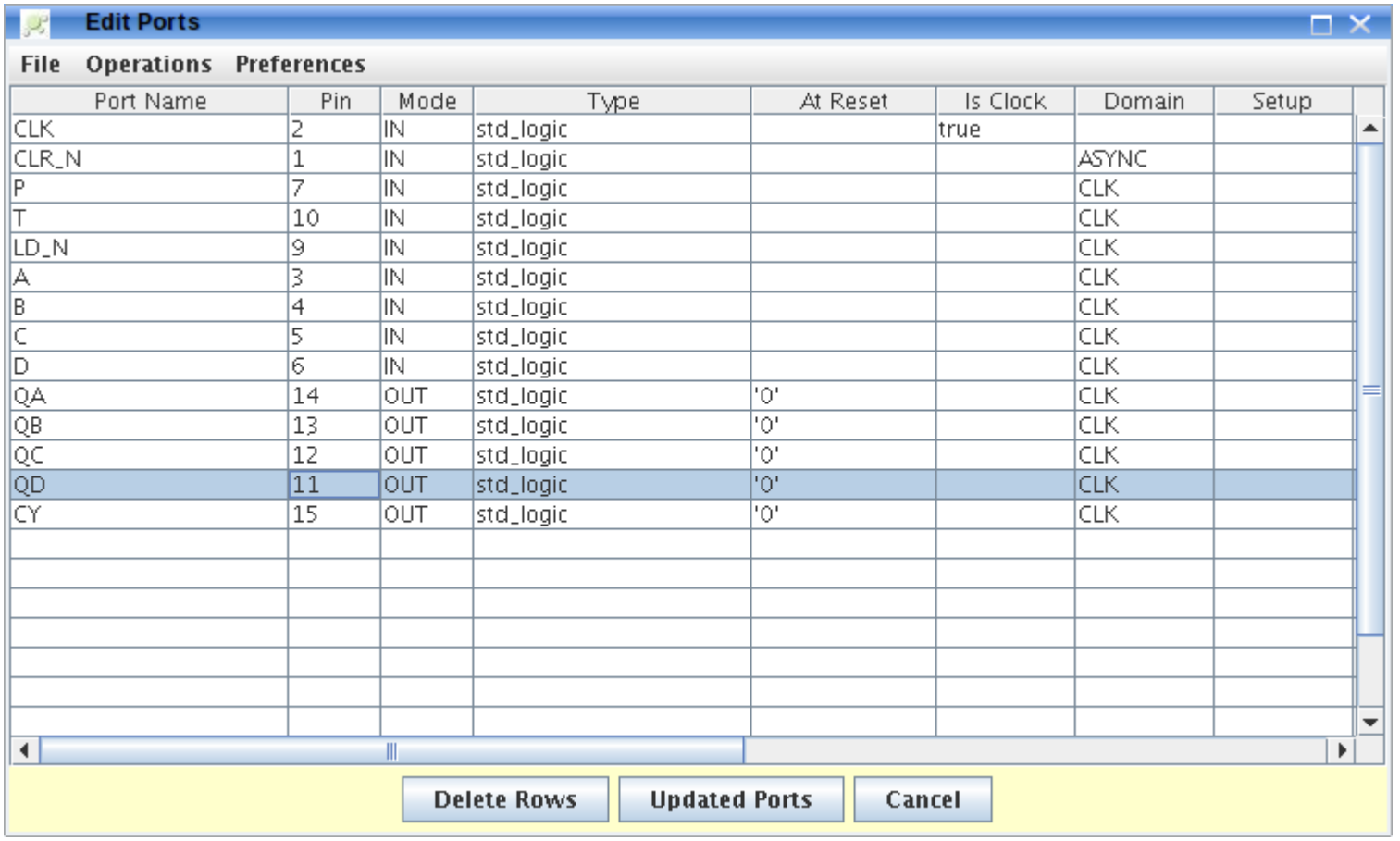


File > Import and select your file

Right click Ports and select Edit Ports



Fill in the Pin column

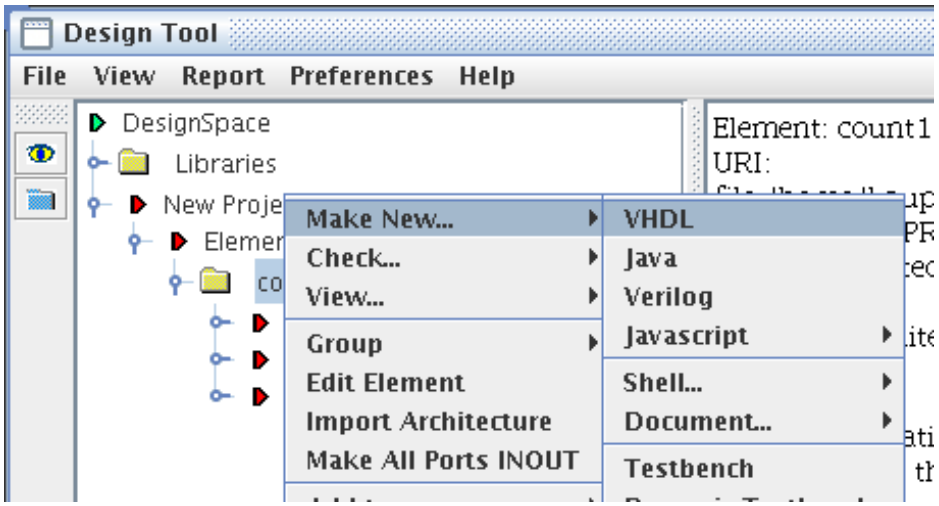


Port Name	Pin	Mode	Type	At Reset	Is Clock	Domain	Setup
CLK	2	IN	std_logic		true		
CLR_N	1	IN	std_logic			ASYNC	
P	7	IN	std_logic			CLK	
T	10	IN	std_logic			CLK	
LD_N	9	IN	std_logic			CLK	
A	3	IN	std_logic			CLK	
B	4	IN	std_logic			CLK	
C	5	IN	std_logic			CLK	
D	6	IN	std_logic			CLK	
QA	14	OUT	std_logic	'0'		CLK	
QB	13	OUT	std_logic	'0'		CLK	
QC	12	OUT	std_logic	'0'		CLK	
QD	11	OUT	std_logic	'0'		CLK	
CY	15	OUT	std_logic	'0'		CLK	

Then click the Updated Ports button.

Make the VHDL file

Right click the top Element and select Make New > VHDL



The entity of the VHDL file will include the pin information.

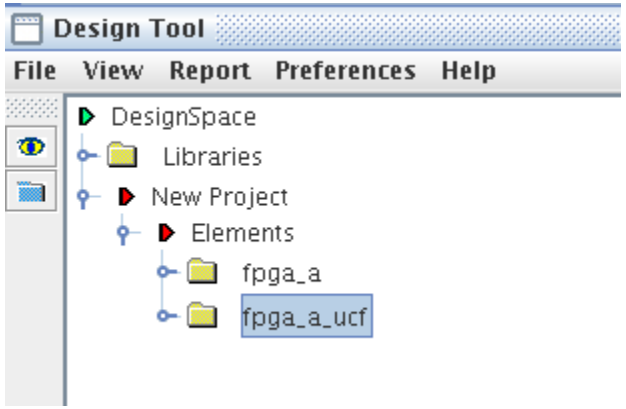
```
ENTITY count161 IS

GENERIC(
     Td    : Time := 2 ns;
     PHYSICAL_PIN_MAP    : String := "PKG_PINS"
     );

PORT(
     CLK    : IN std_logic;    -- rising edge clock
  .....
    CY    : OUT std_logic     -- carry out
     );

SUBTYPE PIN_MAP_STRING IS STRING;

CONSTANT PKG_PINS : PIN_MAP_STRING :=
"CLK : 2," &
"CLR_N : 1," &
"P : 7," &
"T : 10," &
"LD_N : 9," &
"A : 3," &
"B : 4," &
"C : 5," &
"D : 6," &
"QA : 14," &
"QB : 13," &
"QC : 12," &
"QD : 11," &
"CY : 15";

END count161;
```

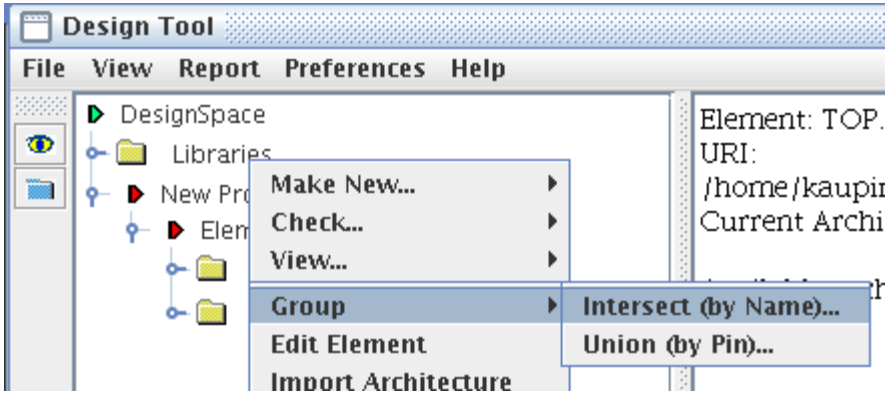
For FPGAs you can import .ucf data

- First read in the design: File > Import File
- Then read the FPGA's ucf file that has pin numbers included: File > Import File

- Select (left click) the ucf Element then select the top FPGA Element
- Right click and select Group > Intersect (by Name)

- Click the Intersect button in the pop-up dialog



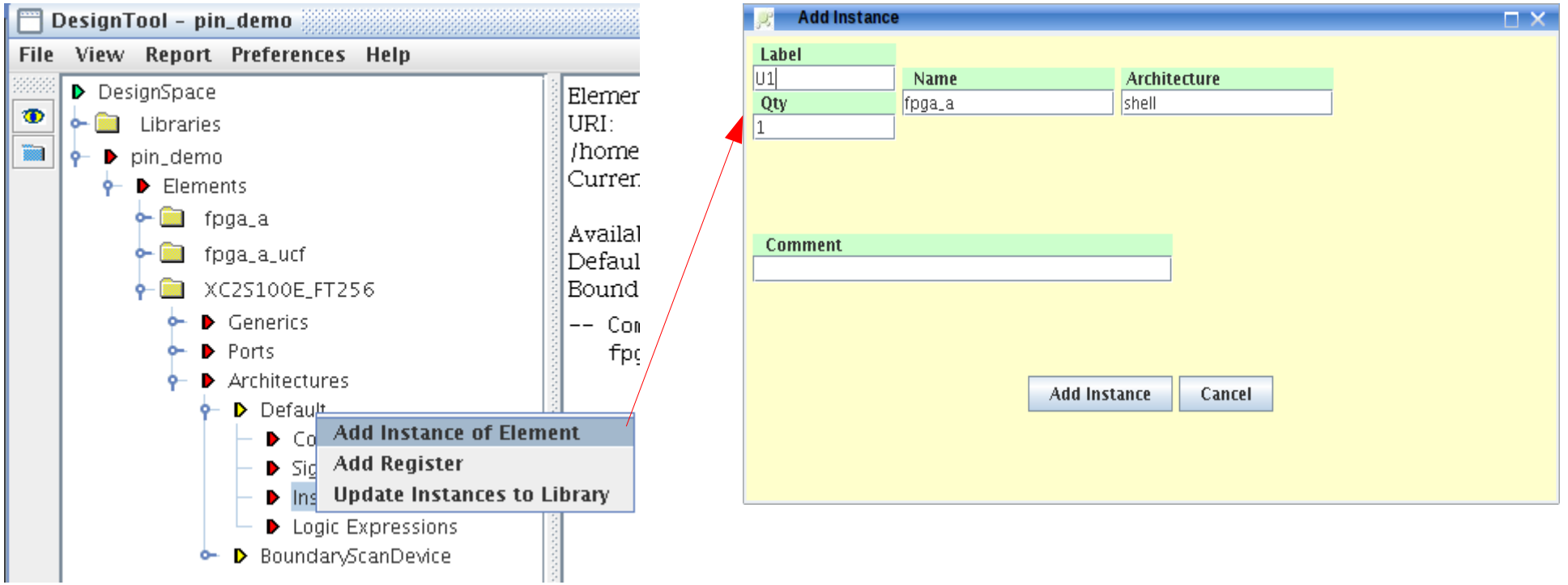


The pin number information will now be transferred to the FPGA design

To add the other package pins...

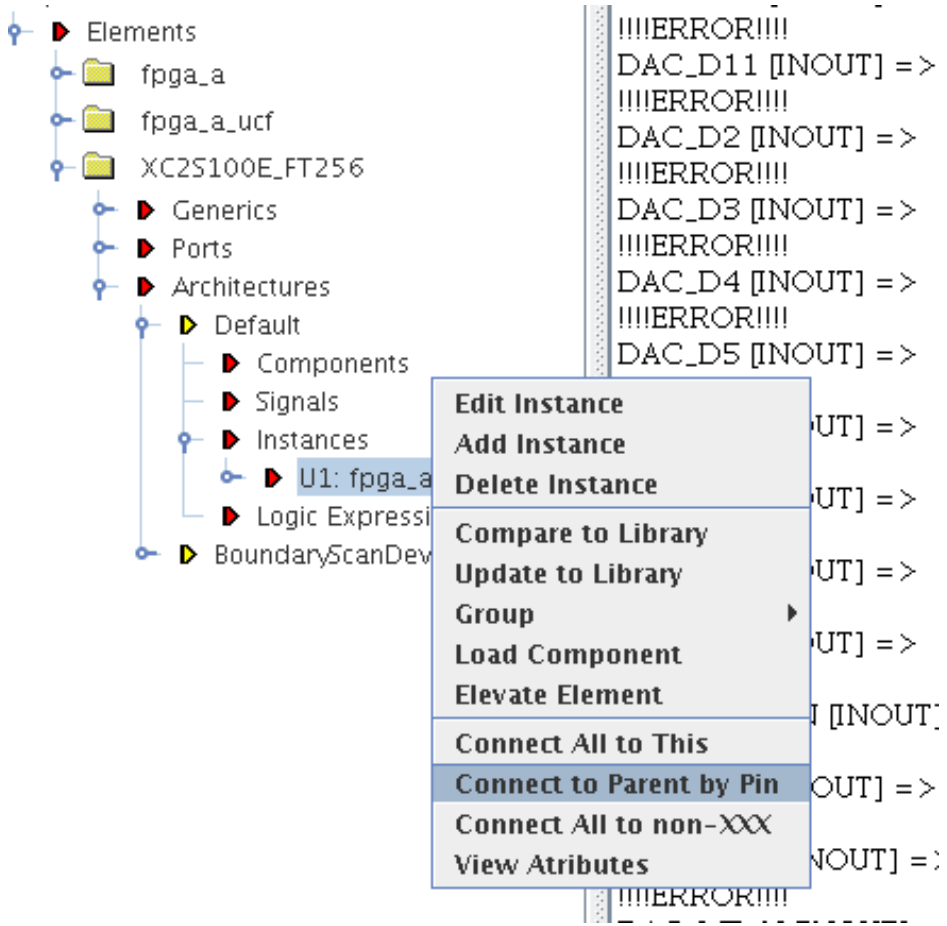
- To add the unused, power, ground and dedicated pins to the design
  - File > Import the vendor's BSDL file
    - Respond YES to Convert Bit to Std_Logic dialog
  - Select (left click) the BSDL Element
  - Left then right click the FPGA Element and select Group > Union (by pin)
    - This adds the remaining package pins to the design
    - A side effect is that it adds an instance of the BSDL Element to the design, but you can select that Instance and Delete it.

or... put the FPGA in the BSDL package



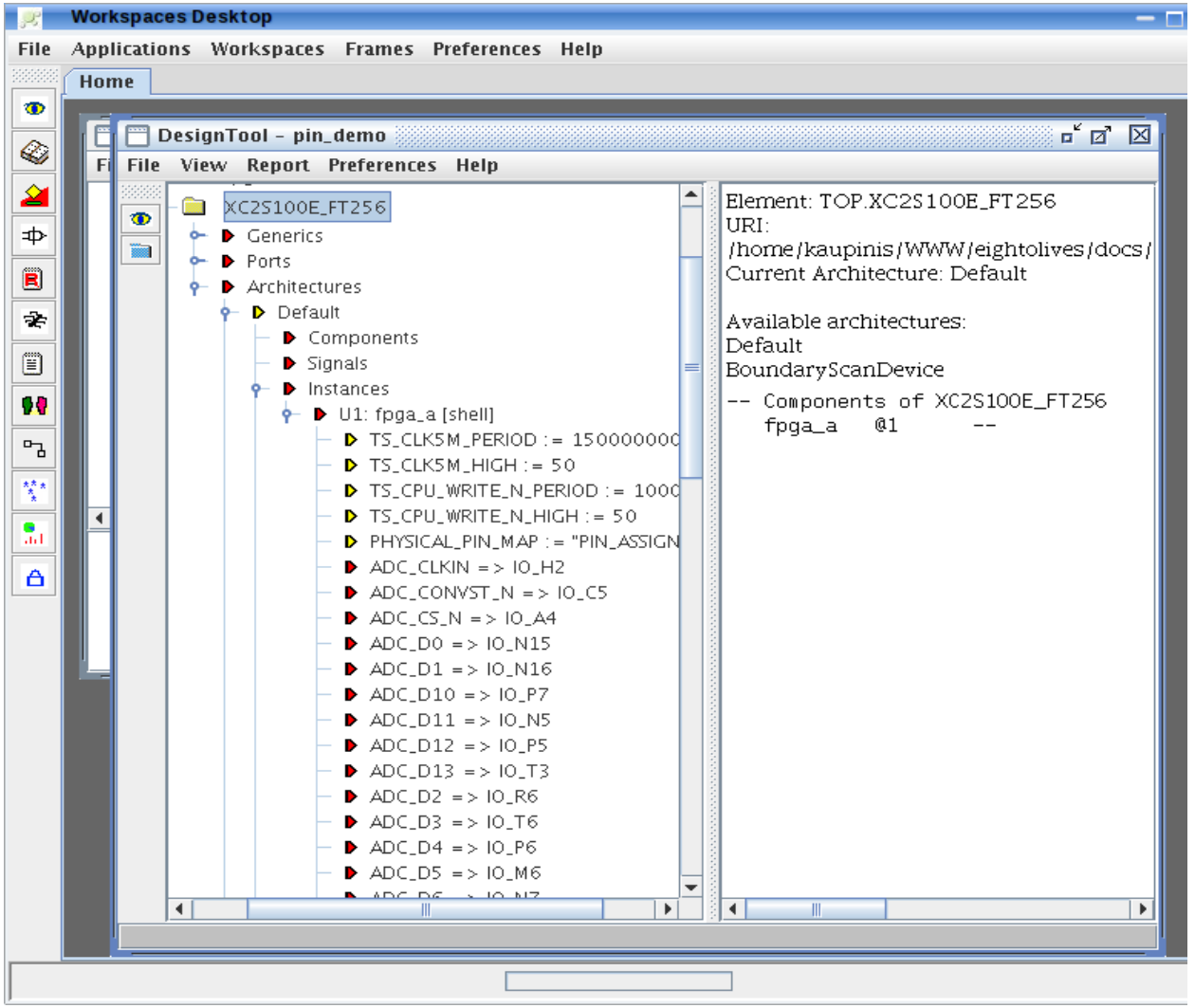
- In the BSDL tree, right click the Default Architecture and select Use This Architecture
- Left click the FPGA Element then right click Instances within the BSDL tree
- Select Add Instance of Element and in the pop-up window add the label “U1”
- Click the Add Instance button

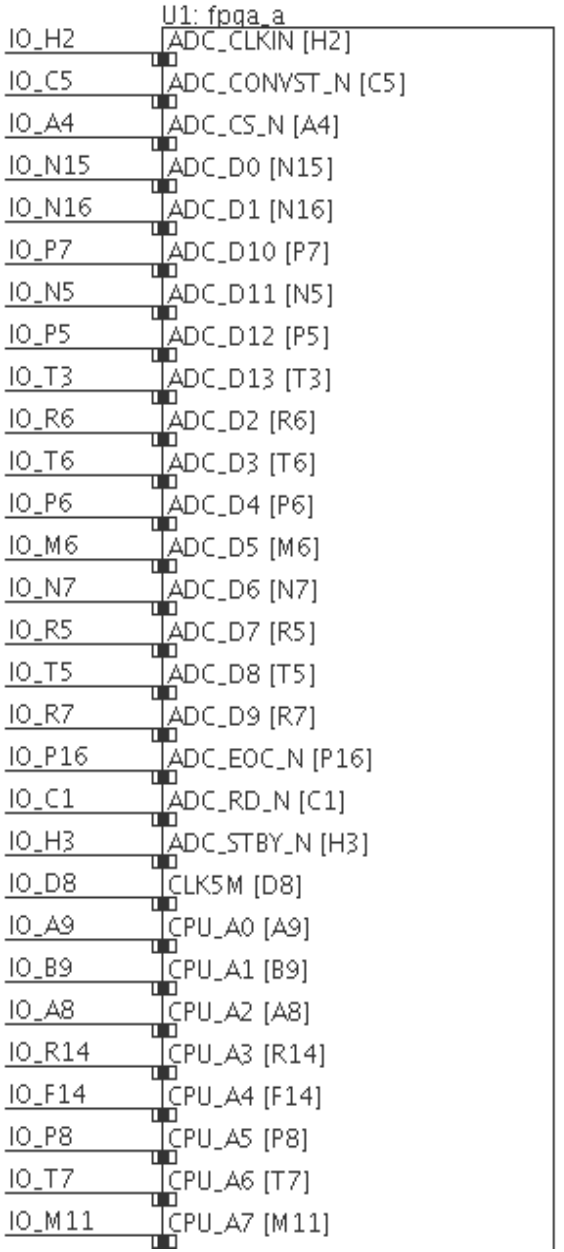
Now we connect U1



- Right click the instance U1 and select Connect to Parent by Pin
- The FPGA will now be connected to the BSDL top Element.
- Right click the BSDL Element and select Make New > VHDL
- Save it.

End result: FPGA connected to BSDL package





VHDL generated from eightolives' Schematic

- A schematic normally uses component symbols that have pin numbers assigned.
- Generating VHDL using eightolives' Schematic will add two generics to an instantiated component:
  - PHYSICAL_PIN_MAP : STRING := “PKG_PINS”;
    - This defines which package to use. Other example: “SOP16”
  - PKG_PINS : PIN_MAP_STRING := "CLK : 4, CLK_N : 5, GND : 3," & "NC : 1, OE : 2, SCL : 8, SDA : 7,VDD : 6";
    - This defines the pin name : pin number pairs

For more information

- Check the tutorials at: http://www.eightolives.com/tutorials.htm
  - Workspaces Desktop Tool Overview
- Checkout the VHDL resources links at: http://www.eightolives.com/technology.htm
- Read the Workspaces Desktop Users Manual